

ENR-325/325L Principles of Digital Electronics and Laboratory

Xiang Li
Fall 2025

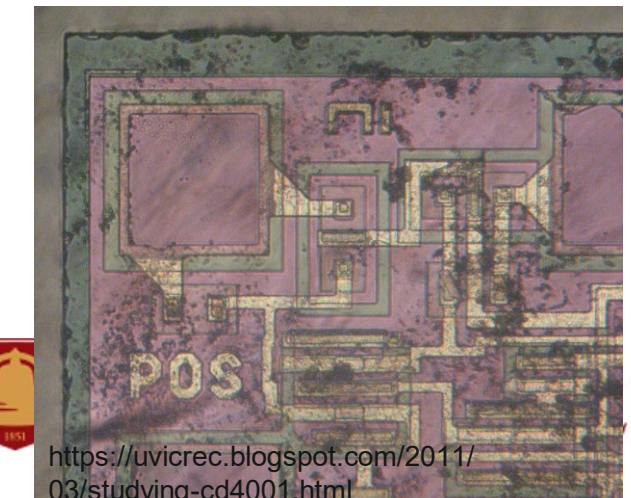
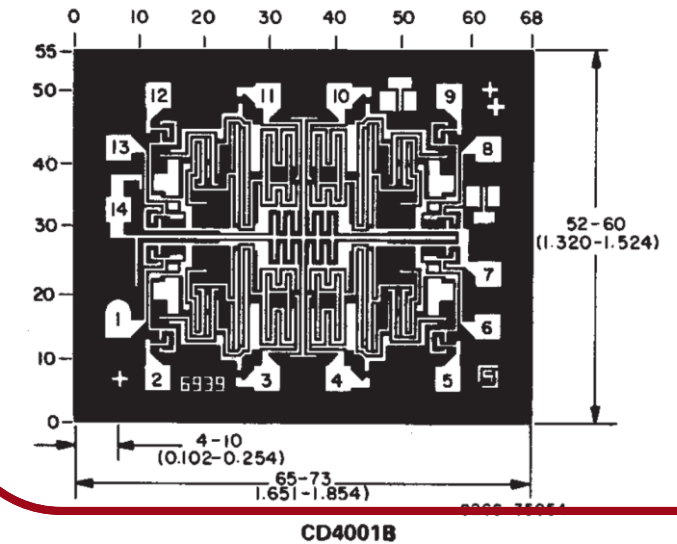
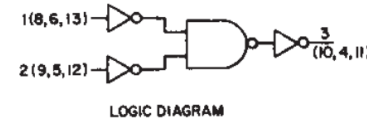
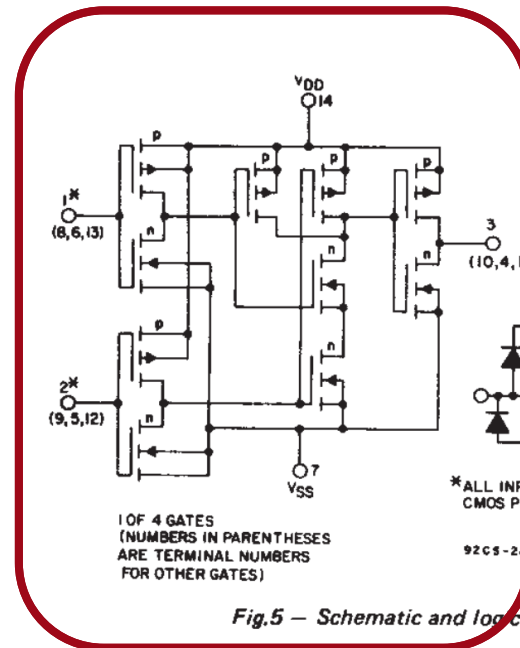
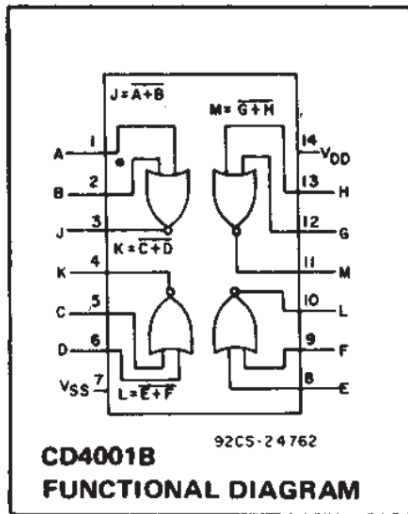
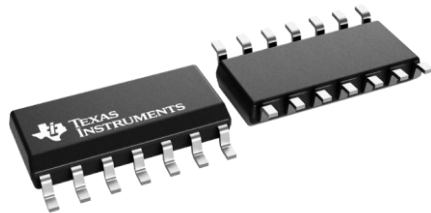
Digital electronics: the multi-staged abstraction:

Application

EE

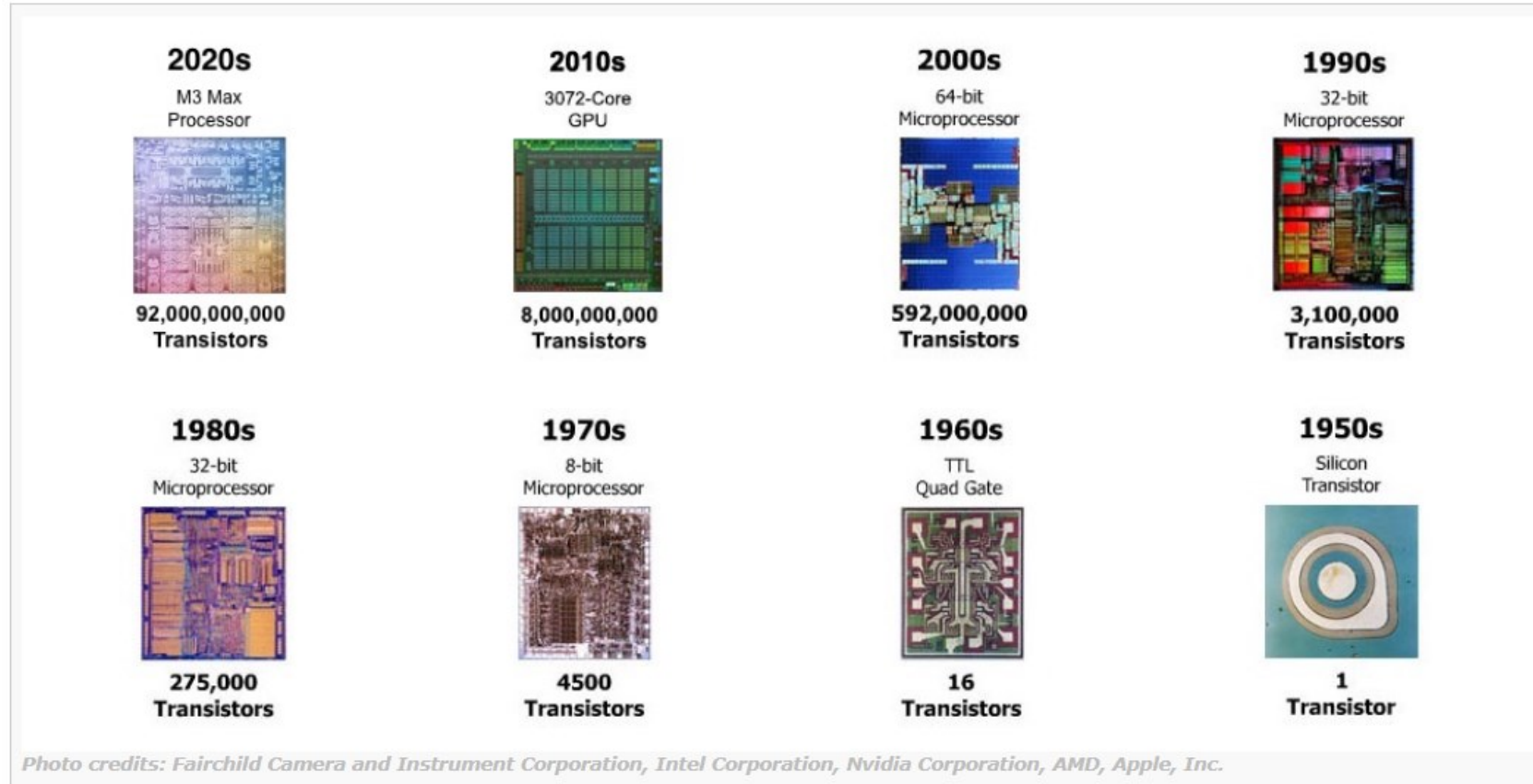
CE

MicroE



GE

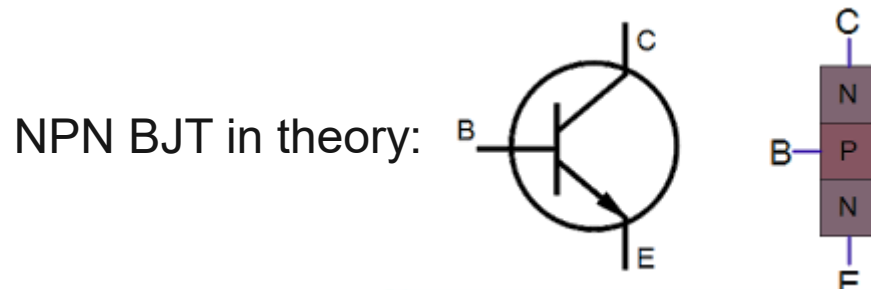
How the arithmetic and logic functions are physically realized



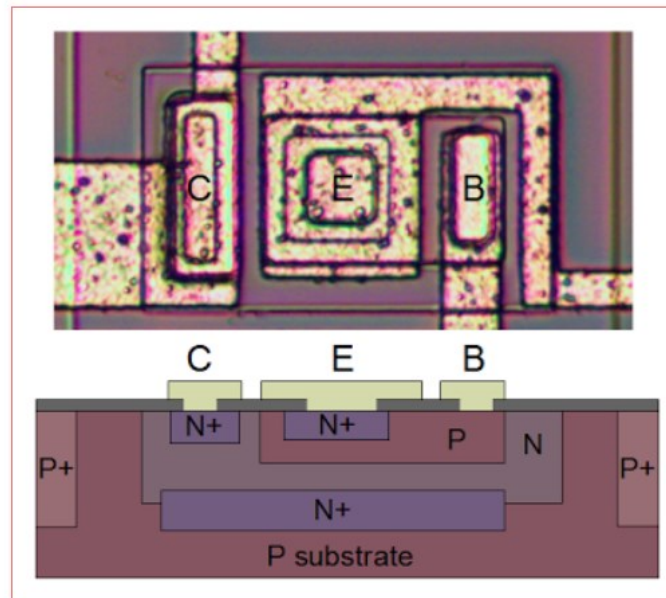
<https://www.computerhistory.org/siliconengine/timeline/>

...and it's very different from the macro world

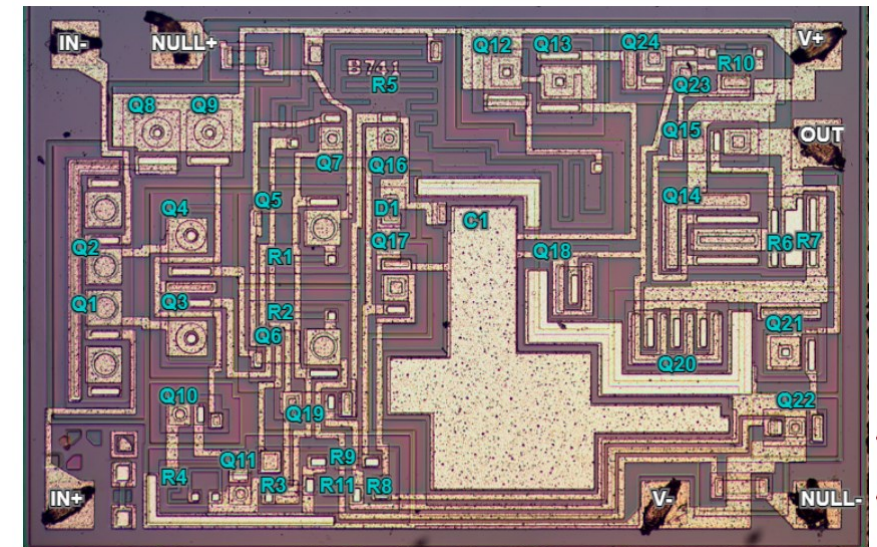
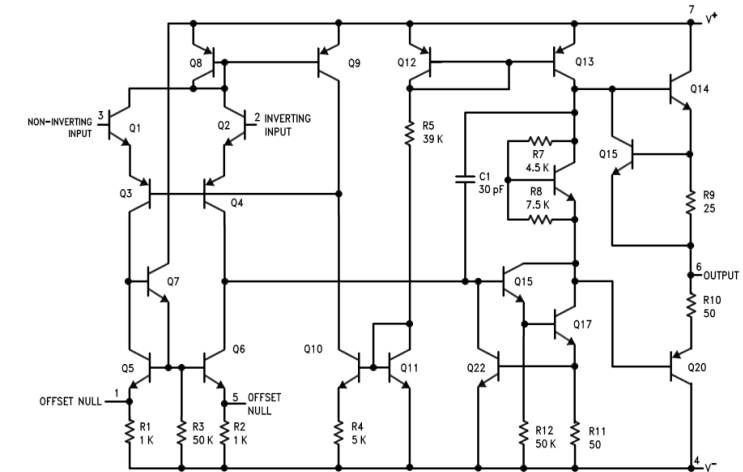
- Example: how op amps chips ACTUALLY works:



NPN BJT in IC:



7.2 Functional Block Diagram



The MOSFET revolution



Robert Noyce, inventor of silicon IC and “mayor of silicon valley”

April 25, 1961

R. N. NOYCE

2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959

3 Sheets-Sheet 2

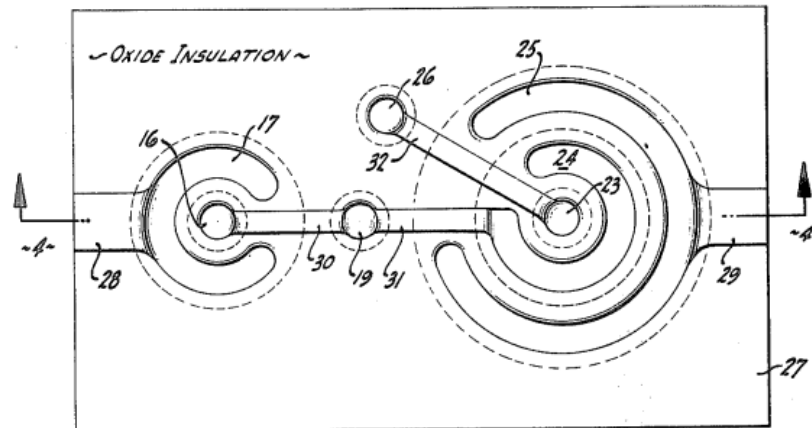


FIG. 3

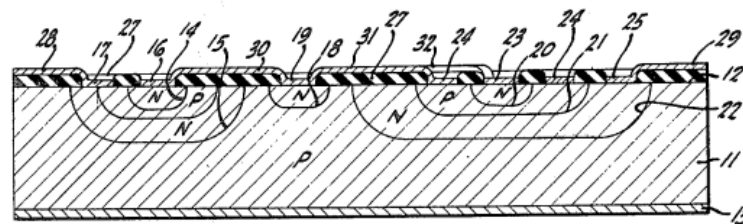


FIG. 4

Aug. 27, 1963

DAWON KAHNG

3,102,230

ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE

Filed May 31, 1960

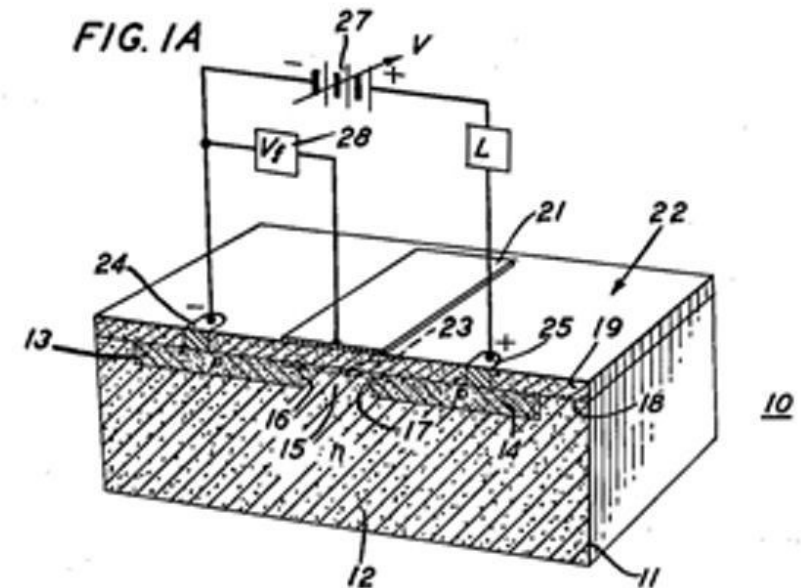
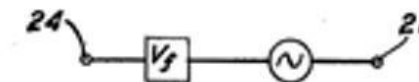


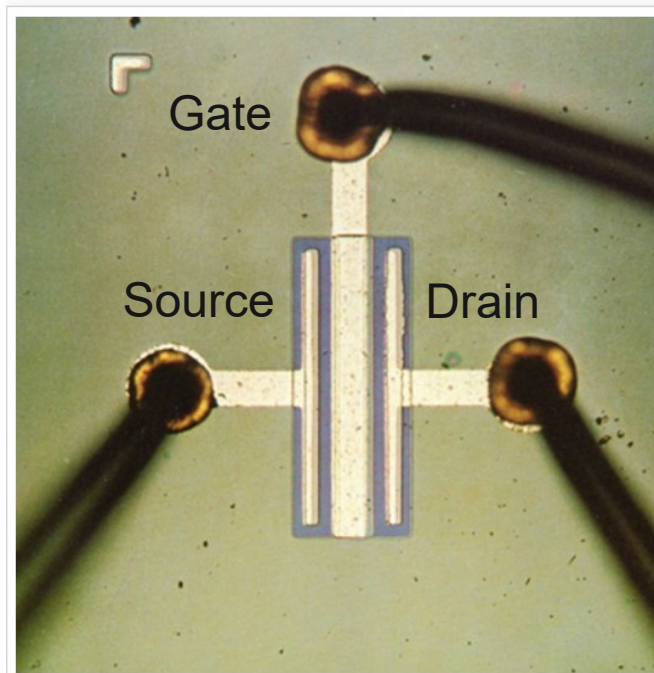
FIG. 1B



Mohamed Atalla and Dawon Kahng's MOS transistor patent. At the time it was 100 times slower than BJT.

The MOSFET revolution

MOS works on “surface physics”:
Solid state, band gap theories,
tunneling effects...



Q Fairchild FI 100 p-channel MOS switching transistor
Credit: Fairchild Camera & Instrument Corporation

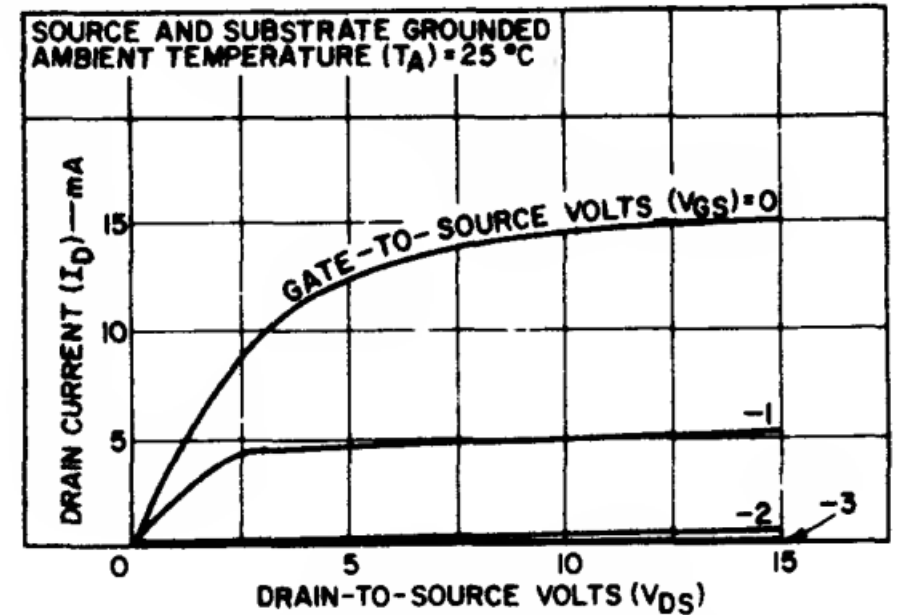


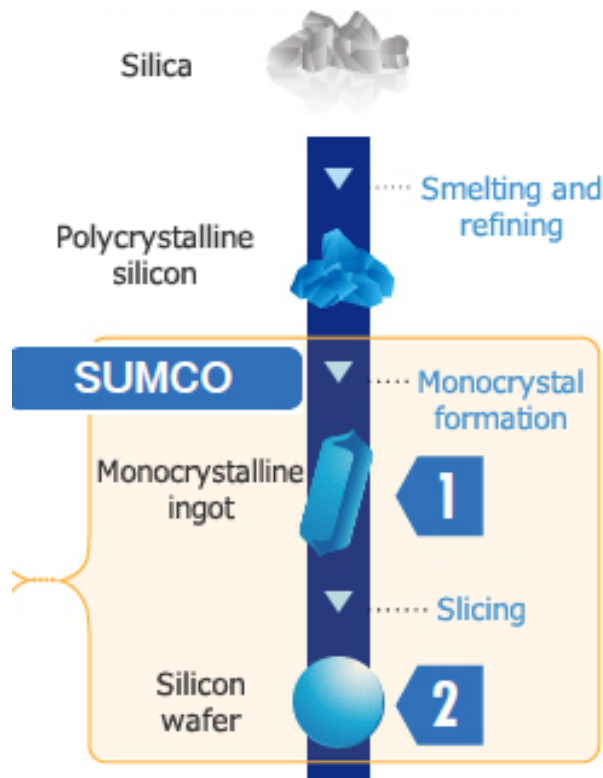
Fig.1 - Transfer characteristics for the RCA 3N128 vhf MOS transistor.

RCA IC and MOSFET Applications Notes, 1983



Bonus slide: how silicon wafer is made

Flow from silicon wafer production to electronic product completion



<https://www.sumcosi.com/>

Czochralski Process



Sliced and polished wafer



Bonus slide: how silicon wafer is sold:

<https://order.universitywafer.com/default.aspx?cat=Silicon>

Qty	ID ↑	Price Per Qty	Diam ↓	Type ↑	Dopant ↑	Orien ↑	Res (Ohm-cm)	Thick (um)	Polish ↑	Grade ↑
100 ▼	3105	\$11.22	25.4mm	P	B	<100>	.01-.05	500um	DSP	Test
10 ▼	4170	\$92.00	300mm	P	B	<100>	1-100ohm.cm	775um	DSP	Dummy
500 ▼	704	\$10.09	200mm					750um	SSP	MECH

The MOSFET fabrication

It was made with...

Surface modification like photolithography

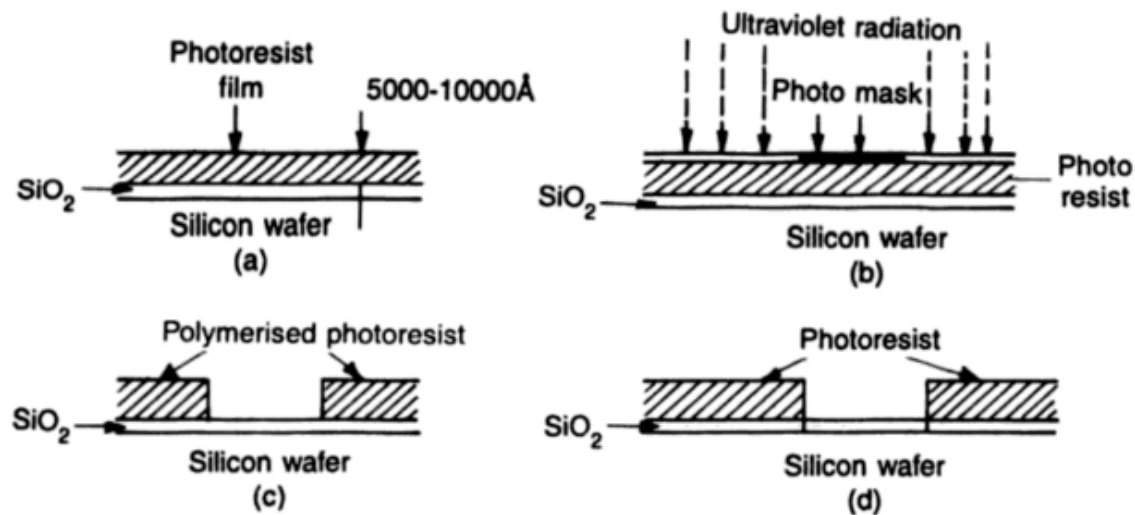


Fig. 1.8 Various steps for photo-etching

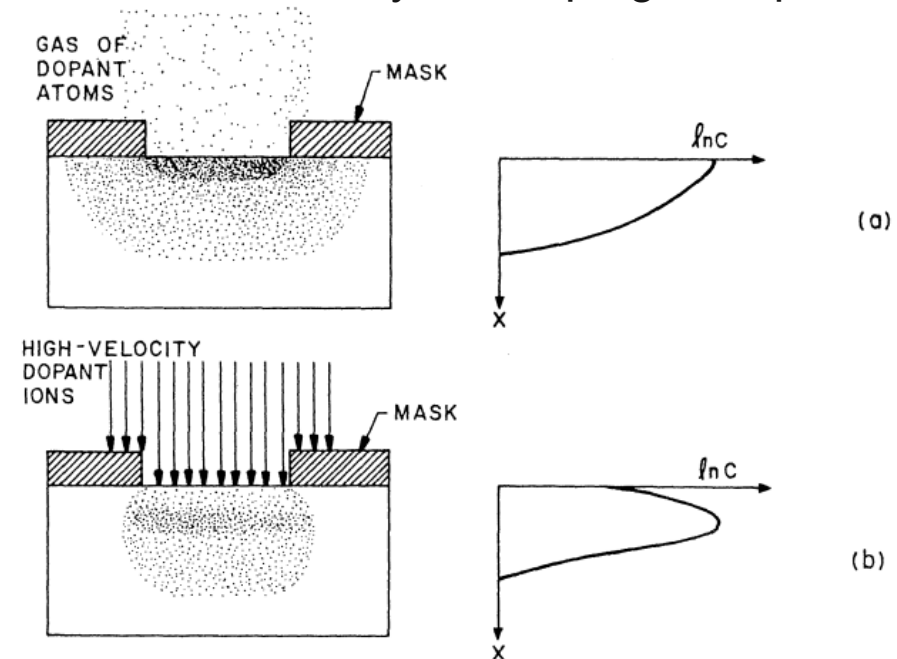
Roy, D. Choudhury. *Linear integrated circuits*. New Age International, 2003.

1 Å = 0.1 nm

1 nm = 0.001 μm

1 μm = 0.001 mm

Surface chemistry like doping of impurities



AP 6120, Chapter 8 Diffusion, CCHK

Why doping?

Because intrinsic silicon is **electrically** uninteresting:

- $\sim 1.08 \times 10^{10}$ electrons turn conductive per cm^3
 - Total electrons: 10^{22}
 - That's one in a trillion odds escaping bonds.
-
- +B to make P type (additional holes h^+)
 - +P to make N type (additional electrons e^-)

5 B Boron	6 C Carbon	7 N Nitrogen
13 Al Aluminium	14 2-8-4 Si Silicon	15 2-8-5 P Phosphorus

Both holes and electrons can be utilized as carriers.

Why doping?

Because intrinsic silicon is **electrically** uninteresting:

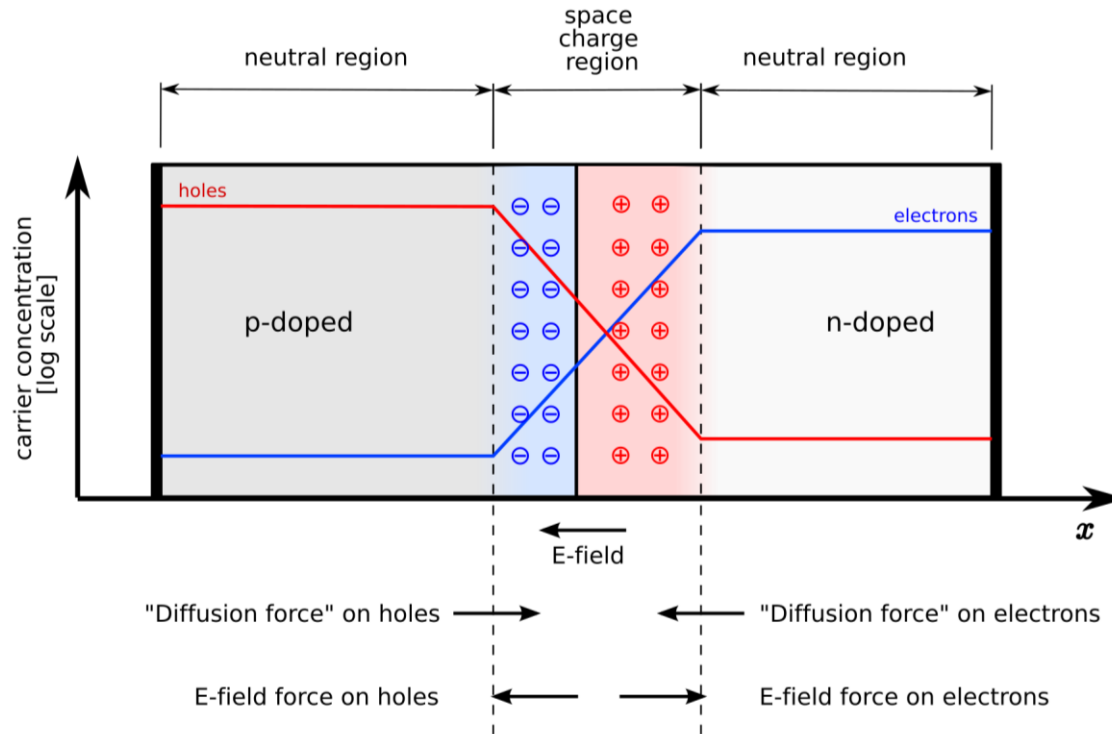
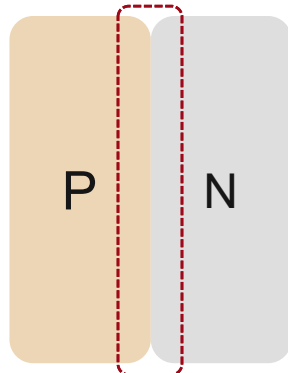
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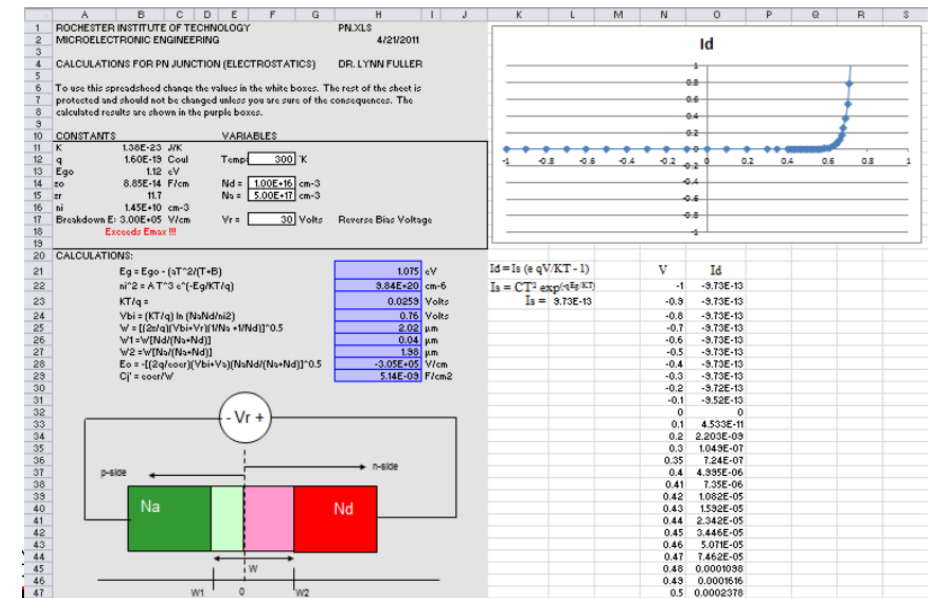
Both holes and electrons can be utilized as carriers.

Empirical Device Models

Diode



https://en.wikipedia.org/wiki/P%E2%80%93n_junction

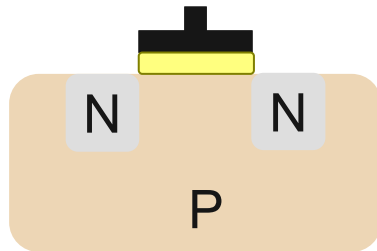


COE COLLEGE

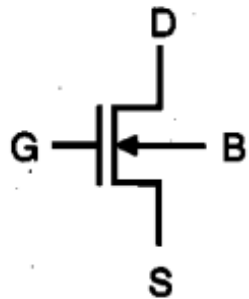
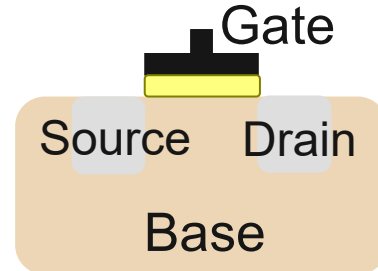
MOSFET is a four terminal system

NMOS

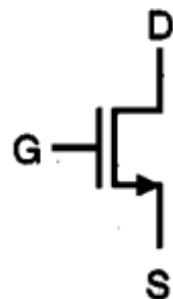
What is doped



What is named



4-Terminal



Simplified

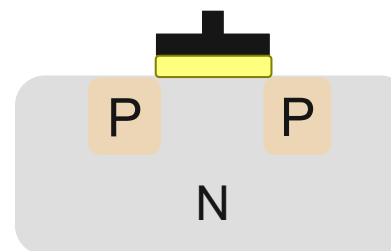


Simplified

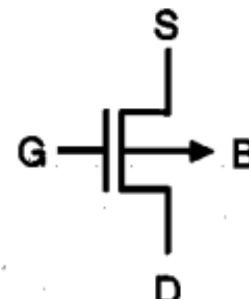
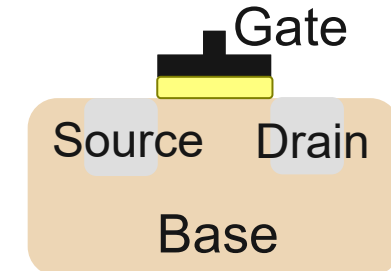
n-channel MOSFET

PMOS

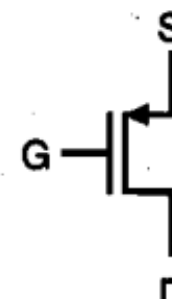
What is doped



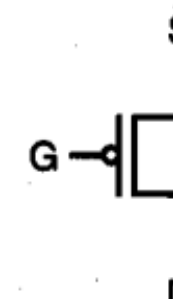
What is named



4-Terminal



Simplified



Simplified

p-channel MOSFET

COLLEGE

And its symbol system is quite confusing, all above are all legit in IEEE standard.

MOSFET physics is complicated

By adjusting doping level:

Enhancement mode: when gate is zero-bias, no conductive channel region.

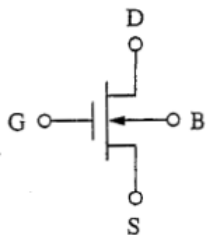
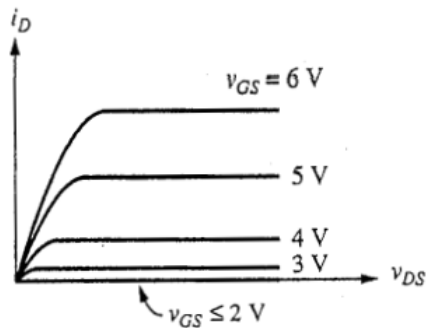
This is the “normally off” condition.

Depletion mode: when gate is zero-bias, already has a conductive channel region.

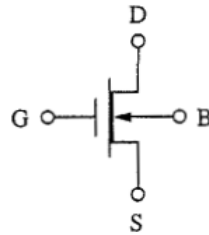
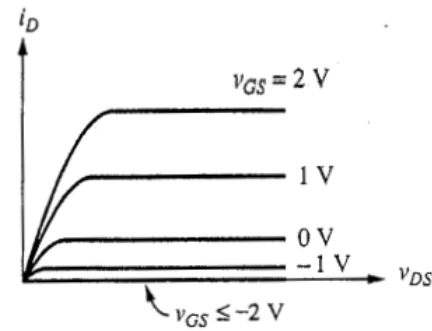
I.e., the “normally on” condition.

NMOS

Enhancement mode

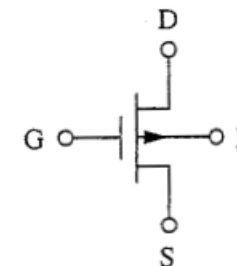
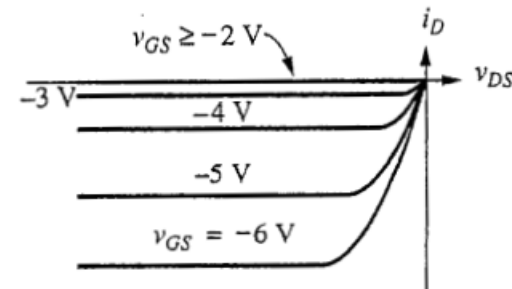


Depletion mode

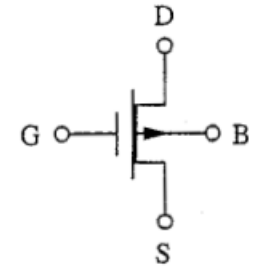
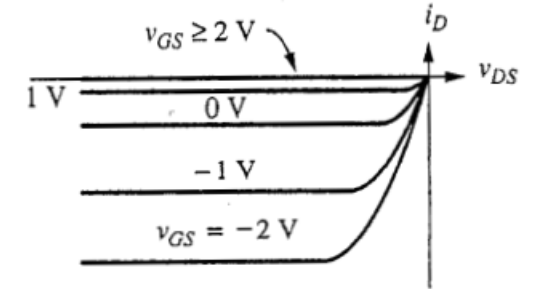


PMOS

Enhancement mode

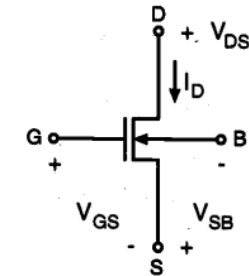
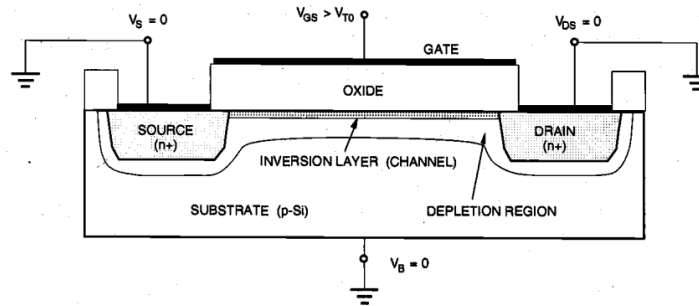
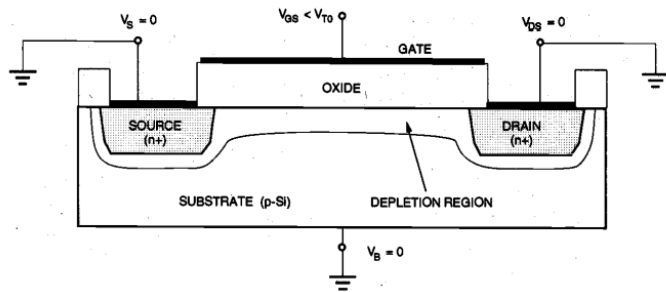


Depletion mode



MOSFET physics is complicated, more example

Four terminal means many bias arrangements (but mostly we manipulate V_{GS} and V_{DS}):



n-channel MOSFET

Current-voltage equations of the n-channel MOSFET :

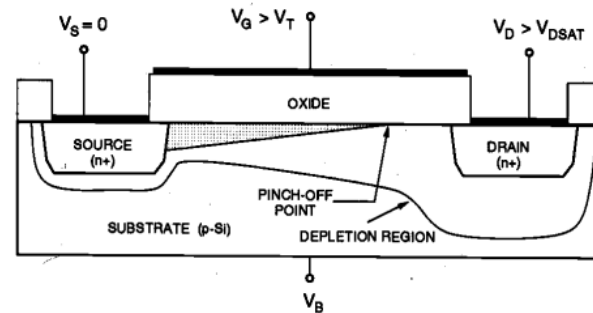
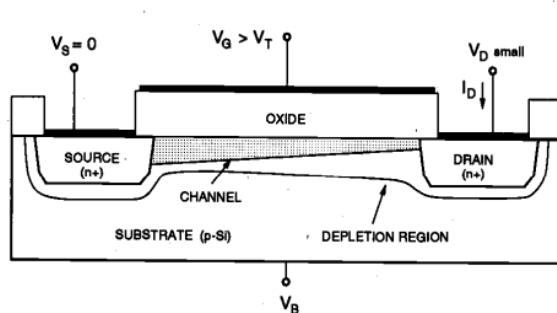
$$I_D = 0, \text{ for } V_{GS} < V_T \quad (3.54)$$

$$I_D(\text{lin}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \text{for } V_{GS} \geq V_T \quad (3.55)$$

and $V_{DS} < V_{GS} - V_T$

$$I_D(\text{sat}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \text{for } V_{GS} \geq V_T \quad (3.56)$$

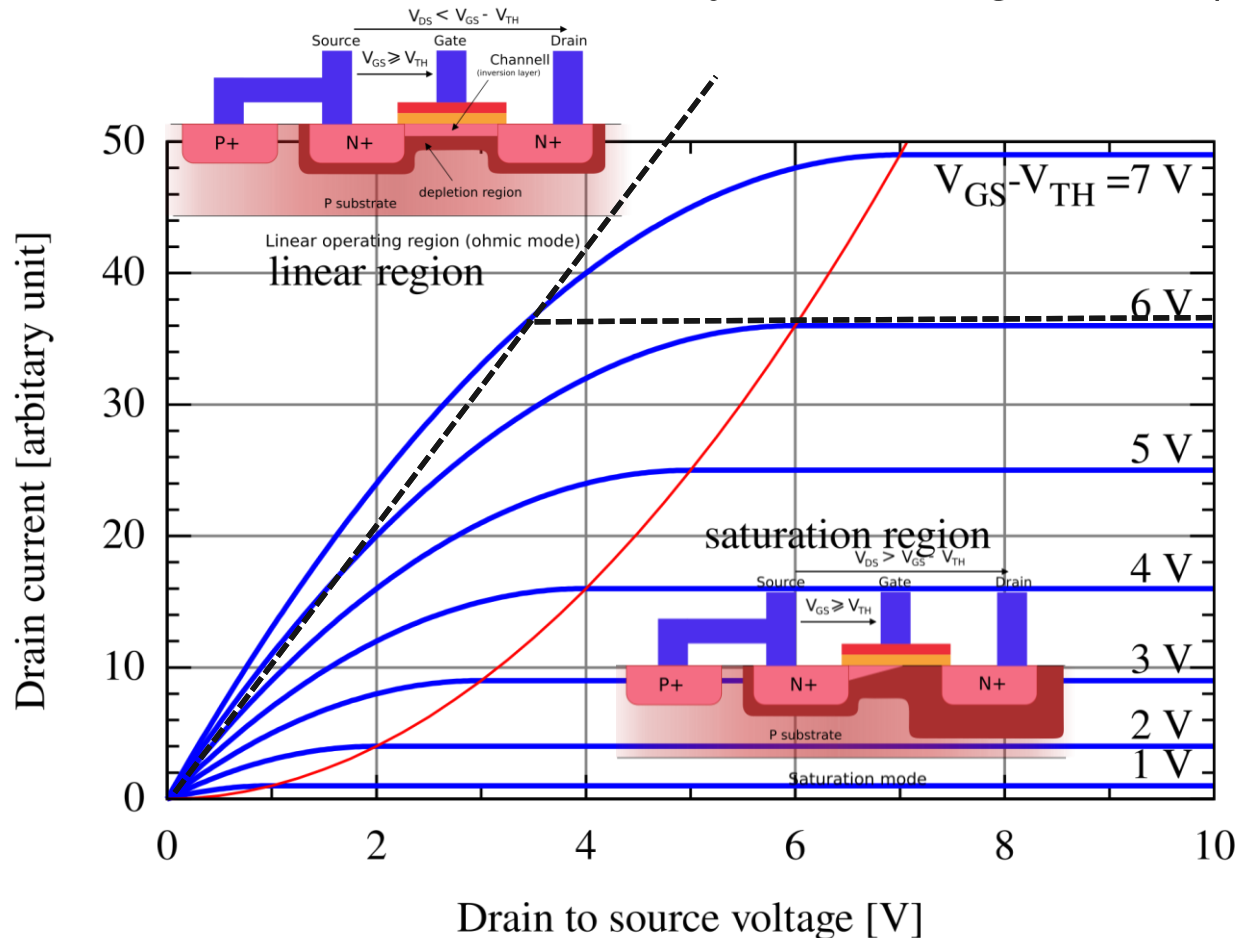
and $V_{DS} \geq V_{GS} - V_T$



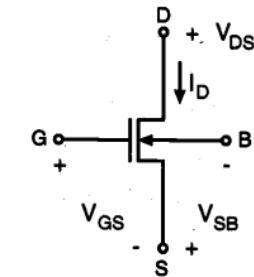
COE COLLEGE

MOSFET physics is complicated, more example

Four terminal means many bias arrangements (but mostly we manipulate V_{GS} and V_{DS}):



<https://en.wikipedia.org/wiki/MOSFET>, this is a simulated graph



n-channel MOSFET

Current-voltage equations of the n-channel MOSFET :

$$I_D = 0, \text{ for } V_{GS} < V_T \quad (3.54)$$

$$I_D(\text{lin}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \text{for } V_{GS} \geq V_T \quad (3.55)$$

and $V_{DS} < V_{GS} - V_T$

$$I_D(\text{sat}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \text{for } V_{GS} \geq V_T \quad (3.56)$$

and $V_{DS} \geq V_{GS} - V_T$

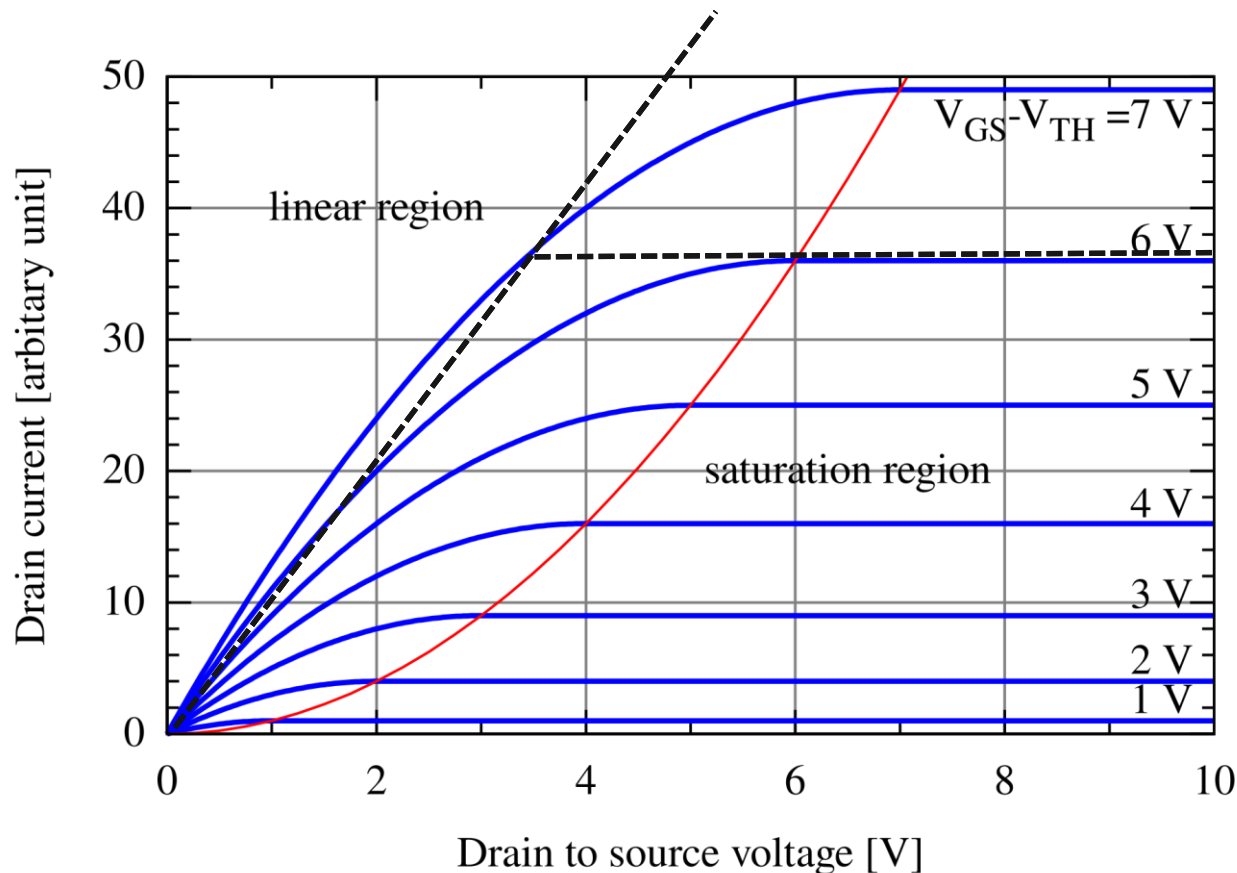


COE COLLEGE

Kang, Sung Mo, and Yusuf Leblebici. *CMOS digital integrated circuits*. New York, NY, USA.: MacGraw-Hill, 2003.

Empirical Device Models

This is a simulated graph



<https://en.wikipedia.org/wiki/MOSFET>

This is a “better” simulated graph

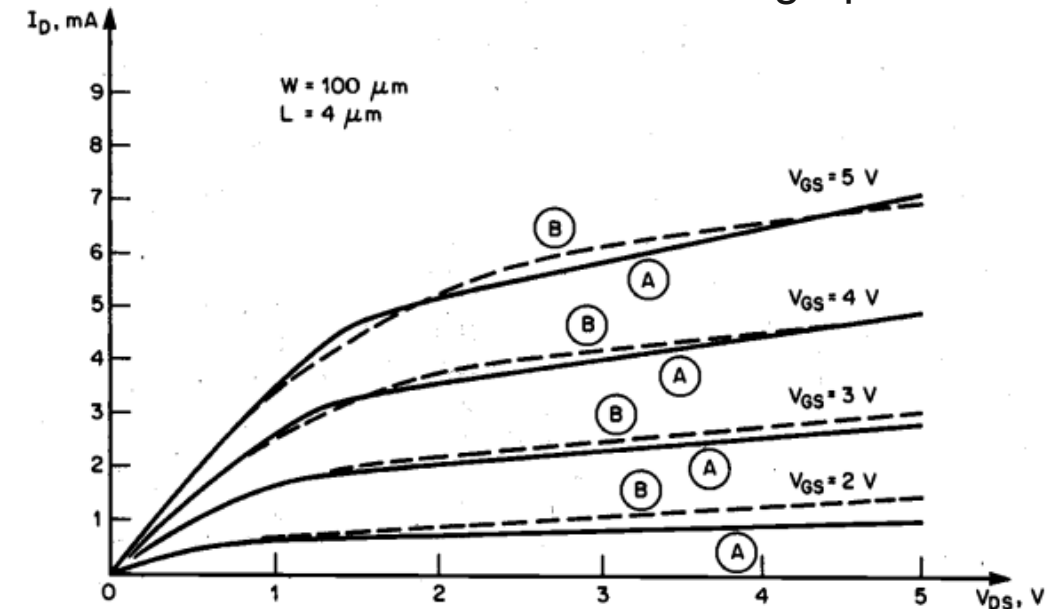


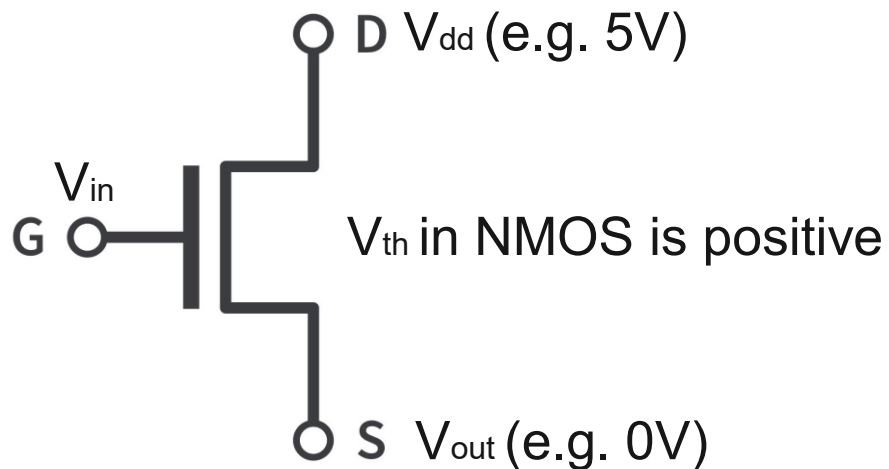
Figure 4.9. Drain current versus drain voltage characteristics of an n-channel MOSFET calculated with the LEVEL 2 model (A) and the LEVEL 3 model (B) (Copyright © 1988 by McGraw-Hill, Inc.).

The parameters common for both models are : $V_{TO} = 1$, $XJ = 1.0\text{E-}6$, $LD = 0.8\text{E-}6$.
The parameters of the LEVEL 2 model are : $UO = 800$, $UCRIT = 5.0\text{E}4$, $UEXP = 0.15$.
The parameters of the LEVEL 3 model are : $UO = 850$, $THETA = 0.04$.

Kang, Sung Mo, and Yusuf Leblebici. *CMOS digital integrated circuits*. New York, NY, USA.: MacGraw-Hill, 2003.

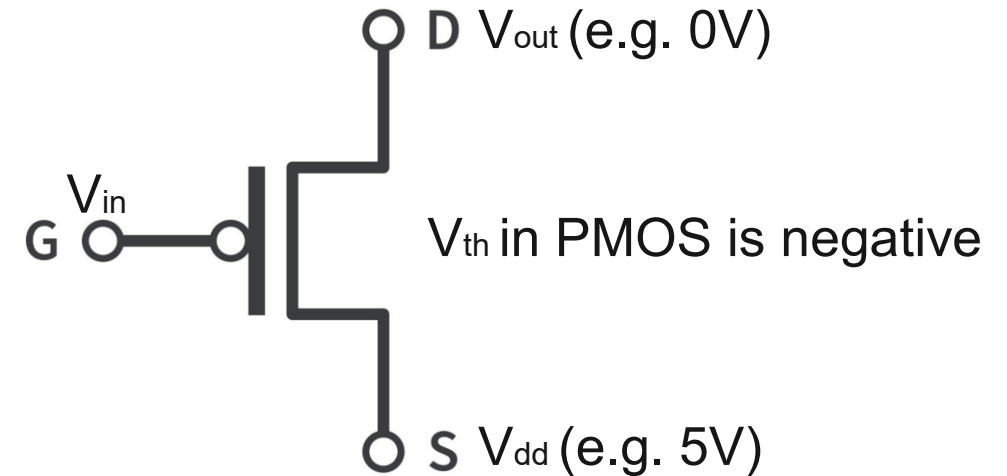
MOSFET as voltage controlled switches:

NMOS as pulldown



Switch	Input
On ($V_{GS} > V_{th}$)	High
Off ($V_{GS} < V_{th}$)	Low

PMOS as pullup

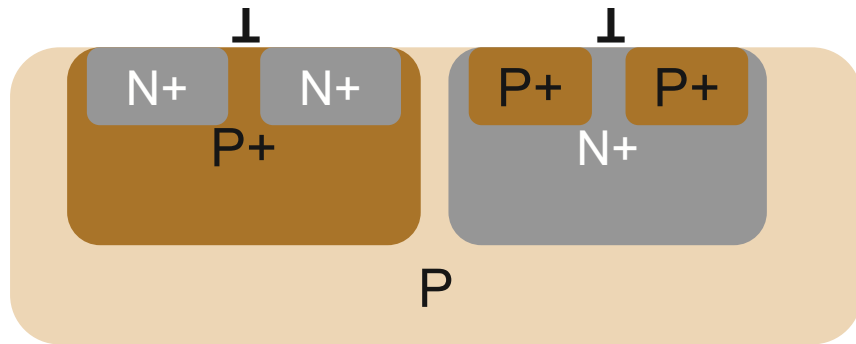


Switch	Input
On ($V_{GS} < V_{th}$)	Low
Off ($V_{GS} > V_{th}$)	High



COE COLLEGE®

Entering the CMOS



Dec. 5, 1967

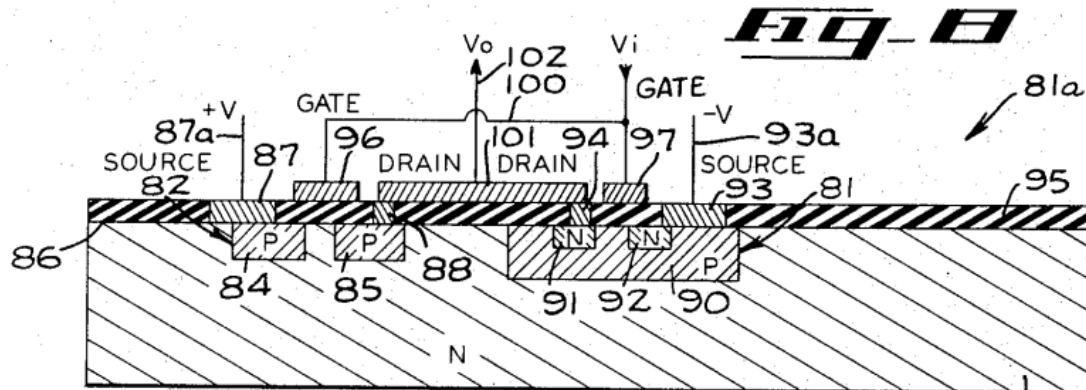
F. M. WANLASS

3,356,858

LOW STAND-BY POWER COMPLEMENTARY FIELD EFFECT CIRCUITRY

Filed June 18, 1963

5 Sheets-Sheet 5



Accordingly, an object of the present invention is to provide circuits in which power losses are minimized.

Another object of the present invention is to provide logic circuits in which power dissipation is reduced during stand-by periods.

Another object of the present invention is to provide a transistor circuit employing field-effect semiconductor devices wherein a field-effect semiconductor device of one carrier type is used as the active load for the field-effect semiconductor device of the opposite carrier type.

Another object of the present invention is to provide a transistor circuit in which an inverter action is produced without employing any passive load element.

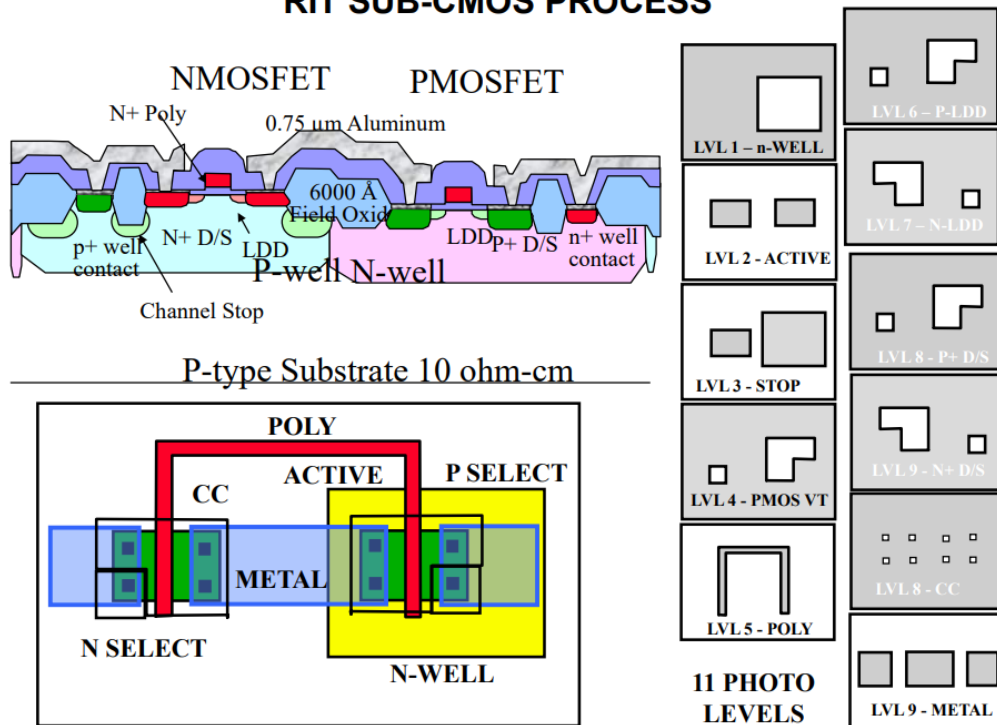


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Entering the CMOS

11 photomasks and 150 fabrication steps, easy!

RIT SUB-CMOS PROCESS



SUB-CMOS 150 PROCESS

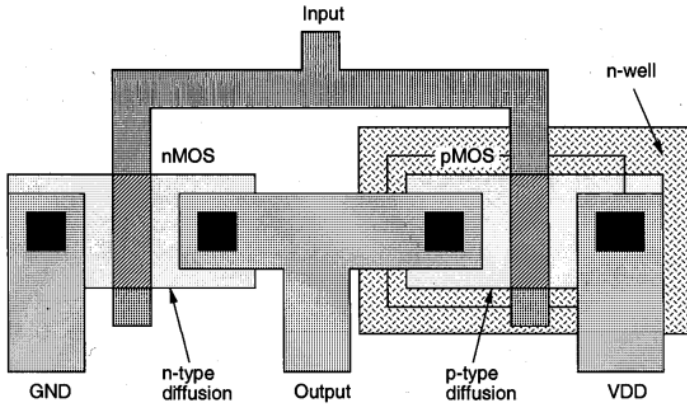
SUB-CMOS Versions 150

- | | | | |
|-------------------------------|-----------------------------|------------------------------|--------------------------------|
| 1. CL01 | 21. IM01- stop | 41. ET07 - Resist Strip | 61. ET26 - CC Etch |
| 2. OX05--- pad oxide, Tube 4 | 22. ET07 Resist Strip | 42. PH03 - 6 - n-LDD | 62. ET07 - Resist Strip |
| 3. CV02- Si3N4-1500Å | 23. CL01 | 43. IM01 | 63. CL01 Special - Two HF Dips |
| 4. PH03 -1- JG nwell | 24. OX04 - field, Tube 1 | 44. ET07 - Resist Strip | 64. ME01 - Metal 1 Dep |
| 5. ET29 - Nitride Etch | 25. ET19 - Hot Phos Si3N4 | 45. PH03 - 7 - p-LDD | 65. PH03 -11- metal |
| 6. IM01 - n-well | 26. ET06 - Oxide Etch | 46. IM01 | 66. ET15 - plasma Etch Al |
| 7. ET07 - Resist Strip | 27. OX04 - Kooi, Tube 1 | 47. ET07 - Resist Strip | 67. ET07 Resist Strip |
| 8. CL01 | 28. IM01 - Blanket Vt | 48. CL01 | 68. SI01 - Sinter |
| 9. OX04 - well oxide, Tube 1 | 29. PH03 - 4-PMOS Vt Adjust | 49. CV03 -TEOS, 5000A | 69. CV03 - TEOS- 4000Å |
| 10. ET19 - Hot Phos Si3N4 | 30. IM01 - Vt | 50. ET10 - Spacer Etch | 70. PH03 - VIA |
| 11. IM01 - p-well | 31. ET07 - Resist Strip | 51. PH03 - 8 - N+D/S | 71. ET26 - Via Etch |
| 12. OX06 - well drive, Tube 1 | 32. ET06 - Oxide Etch | 52. IM01 - N+D/S | 72. ET07 - Resist Strip |
| 13. ET06 - Oxide Etch | 33. CL01 | 53. ET07 - Resist Strip | 73. ME01 - Metal 2 Dep |
| 14. CL01 | 34. OX06 - gate, Tube 4 | 54. PH03 - 9 P+ D/S | 74. PH03- M2 |
| 15. OX05 - pad oxide, Tube 4 | 35. CV01 - Poly 5000A | 55. IM01 - P+ D/S | 75. ET15 - plasma Etch Al |
| 16. CV02 - Si3N4 -1500 Å | 36. IM01 - dope poly | 56. ET07 - Resist Strip | 76. ET07 - Resist Strip |
| 17. PH03 - 2 - JG Active | 37. OX08 - Anneal, Tube 3 | 57. CL01 Special - No HF Dip | 77. SEM1 |
| 18. ET29 - Nitride Etch | 38. DE01 - 4 pt Probe | 58. OX08 - DS Anneal, Tube 2 | 78. TE01 |
| 19. ET07 - Resist Strip | 39. PH03-5-JG poly | 59. CV03 - TEOS, 4000A | 79. TE02 |
| 20. PH03 - Pwell Stop | 40. ET08 - Poly Etch | 60. PH03 - 10 CC | 80. TE03 |



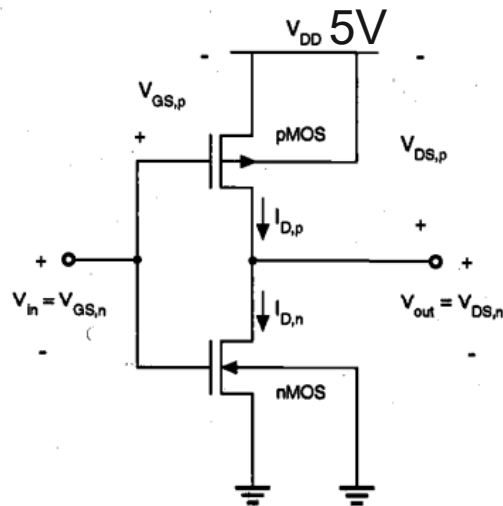
COE COLLEGE

CMOS NOT gate (inverter)

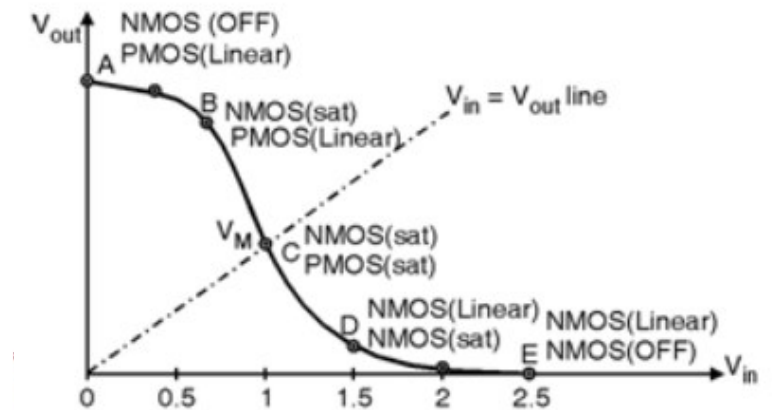
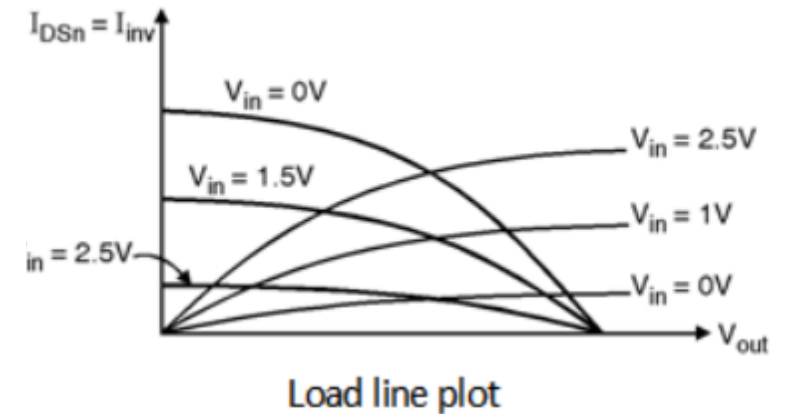
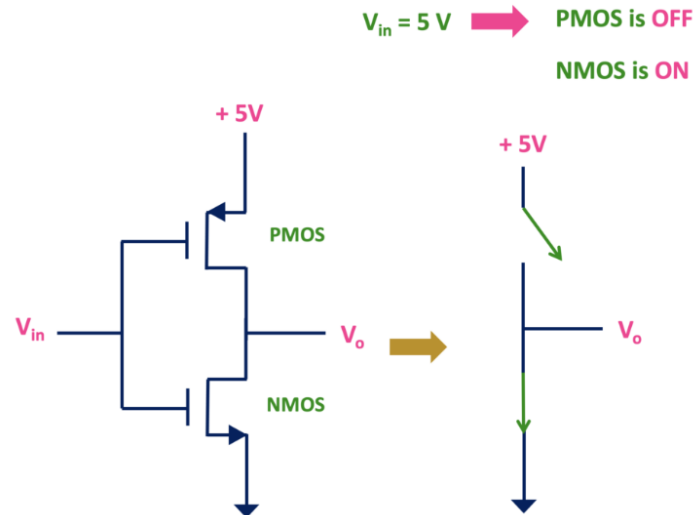
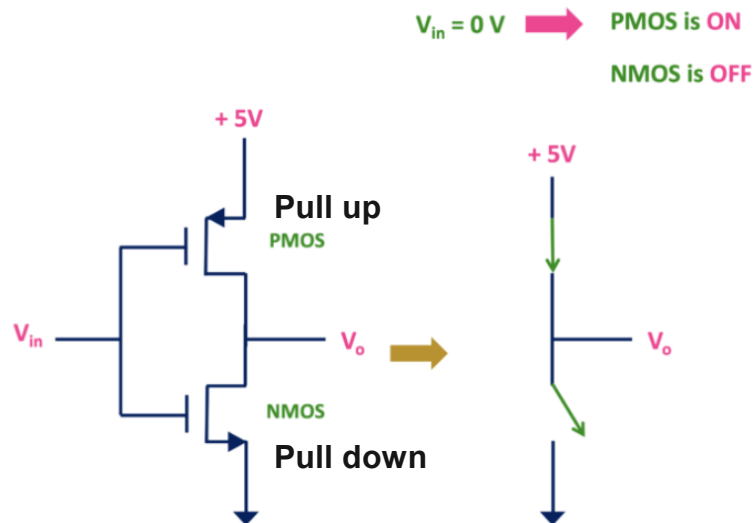


Another object of the present invention is to provide a transistor circuit in which an inverter action is produced without employing any passive load element.

V_{in}	$V_{GS,n}$	$V_{GS,p}$	PMOS	NMOS	V_{out}
0V	0V	-5V	ON	OFF	V_{DD}
5V	5V	0V	OFF	ON	0



No passive load, no power drain in steady state



VTC of CMOS inverter

No passive load, no power drain in steady state

Logic gates can sure be built in other forms, like this all NMOS inverter:

From 1973 Motorola Linear Integrated Circuits Data Book

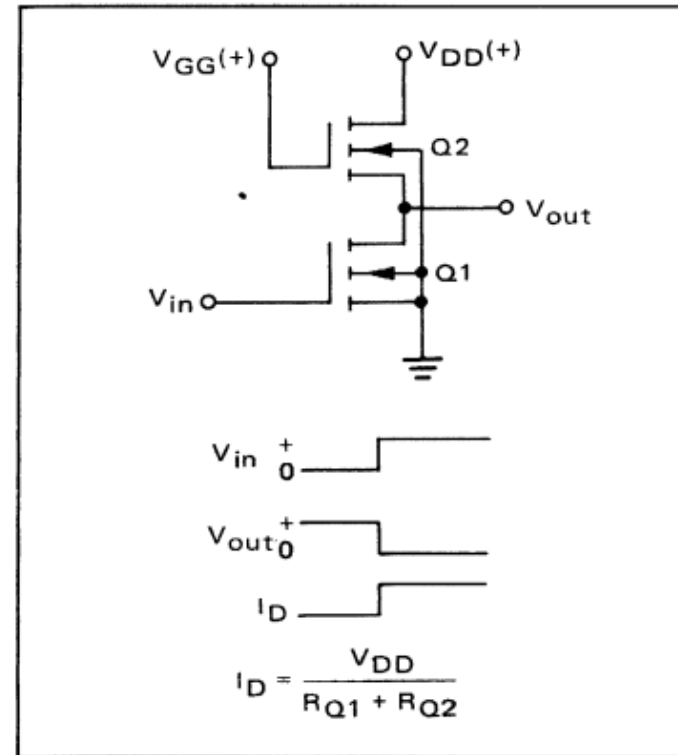


FIGURE 1-3 – TYPICAL N-CHANNEL INVERTER

No passive load, no power drain in steady state

Although CMOS is more complex in structure and fab process, it is more power efficient:

At the end of the day, it's all about:

- Size
- Speed
- Power consumption

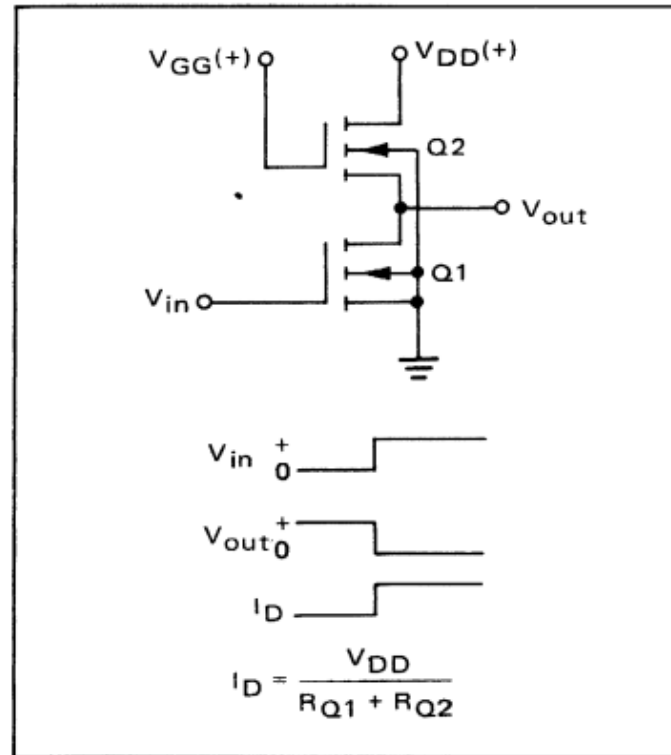


FIGURE 1-3 – TYPICAL N-CHANNEL INVERTER

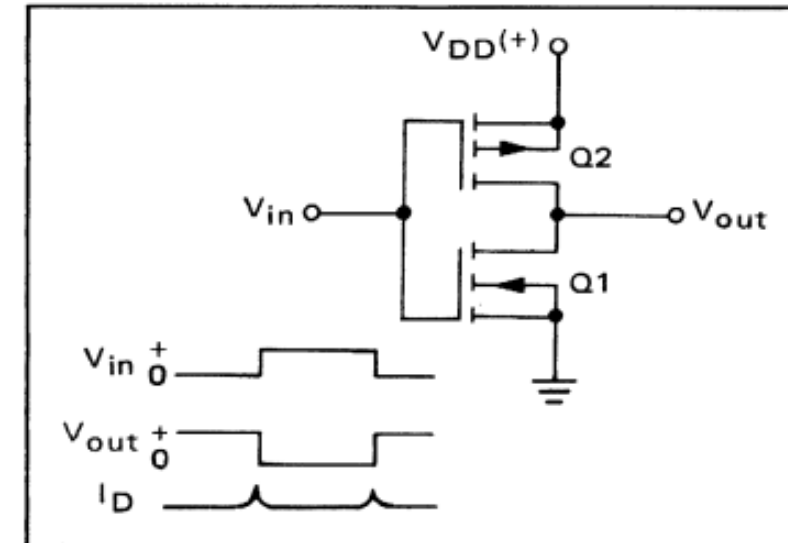


FIGURE 1-4 – TYPICAL COMPLEMENTARY INVERTER



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