ENR-325/325L Principles of Digital Electronics and Laboratory

Xiang Li

Fall 2025

COE COLLEGE

Hamming codes can be done in the EE way

- Before that, we need to acquire some basic skillsets.

Pre-step: Data forms

Step 1: Data manipulation

Step 2: Information storage

Step 3: Interface

3.1 Information flow

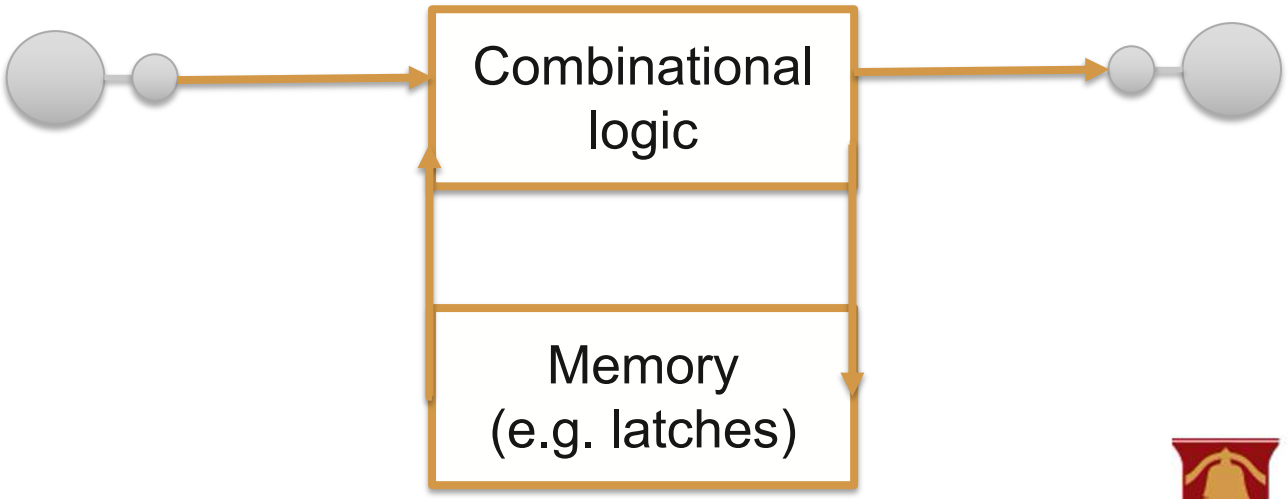
3.2 Physical contacts

COE COLLEGE

3.1 Information flow and sequential logic

- Our previous logic circuits are mostly **combinational.**
- To expand the functions of their finite gates and I/Os, we need to introduce another dimension: **time.**
- It also allows us to **synchronize** the operations when we need to do **iterations (loops)**.

Sequential logic diagram

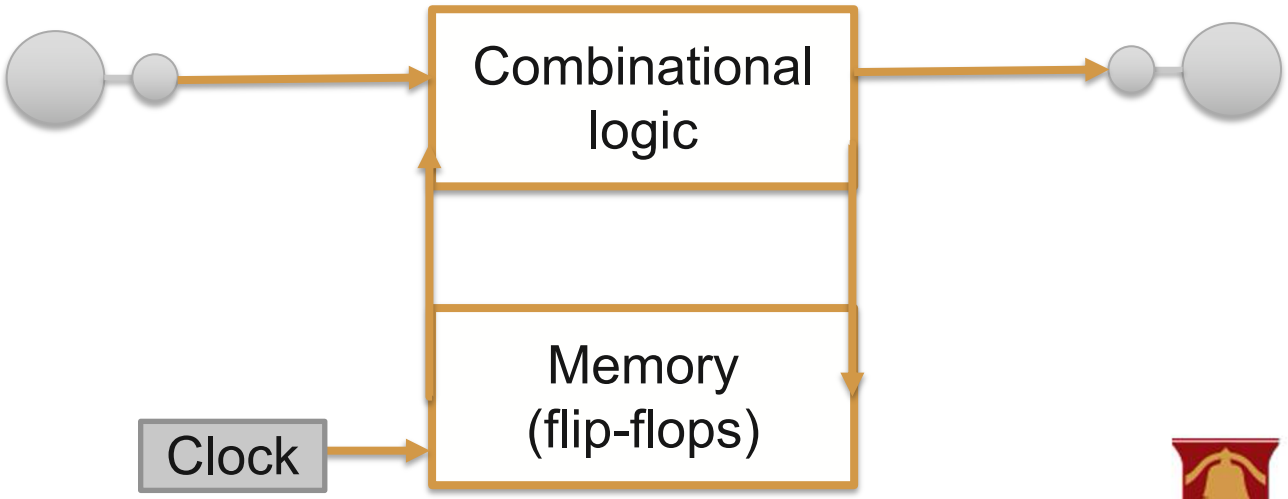


COE COLLEGE

3.1 Information flow and sequential logic

- Our previous logic circuits are mostly **combinational.**
- To expand the functions of their finite gates and I/Os, we need to introduce another dimension: **time.**
- It also allows us to **synchronize** the operations when we need to do **iterations (loops)**.

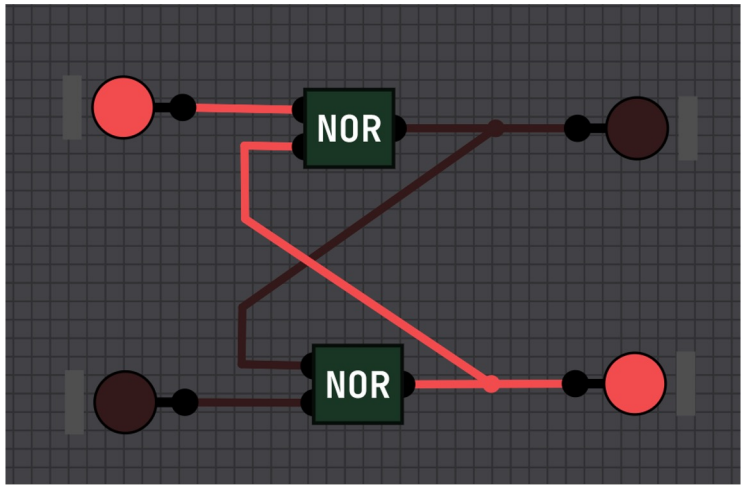
Clocked sequential logic diagram



COE COLLEGE

From latch to flip flop

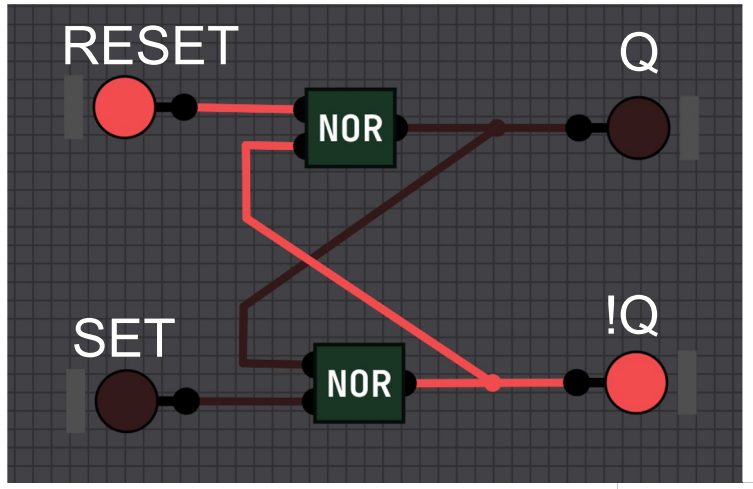
SR latch



COE COLLEGE

Understanding SR latch with truth table and timing diagram

SR latch

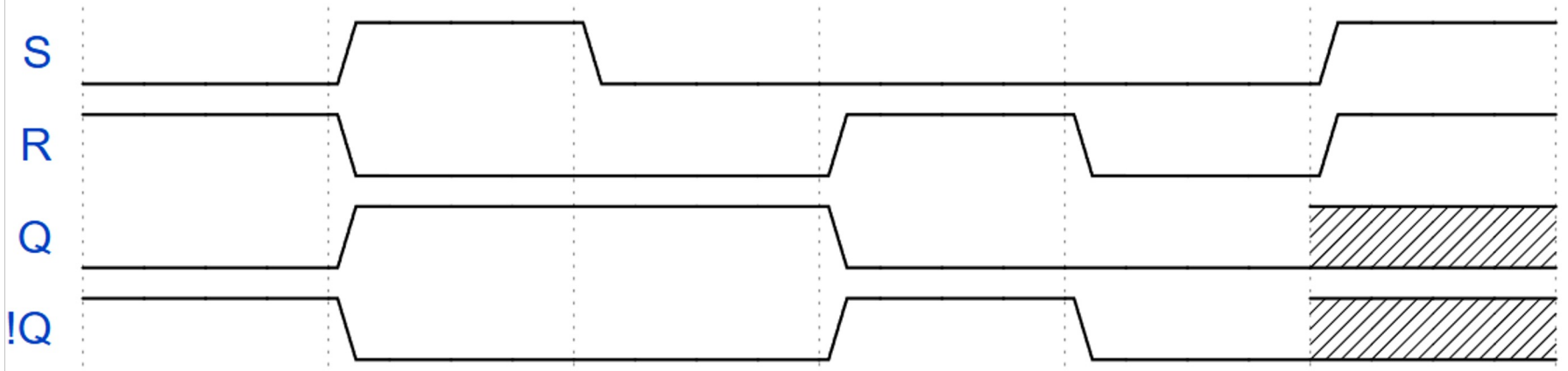


SR latch truth table

S	R	Output (Q)
0	0	**Previous State**
0	1	**0**
1	0	**1**
1	1	**0 (Invalid)**

(HOLD)

SR Latch Timing Diagram (NOR Gates)



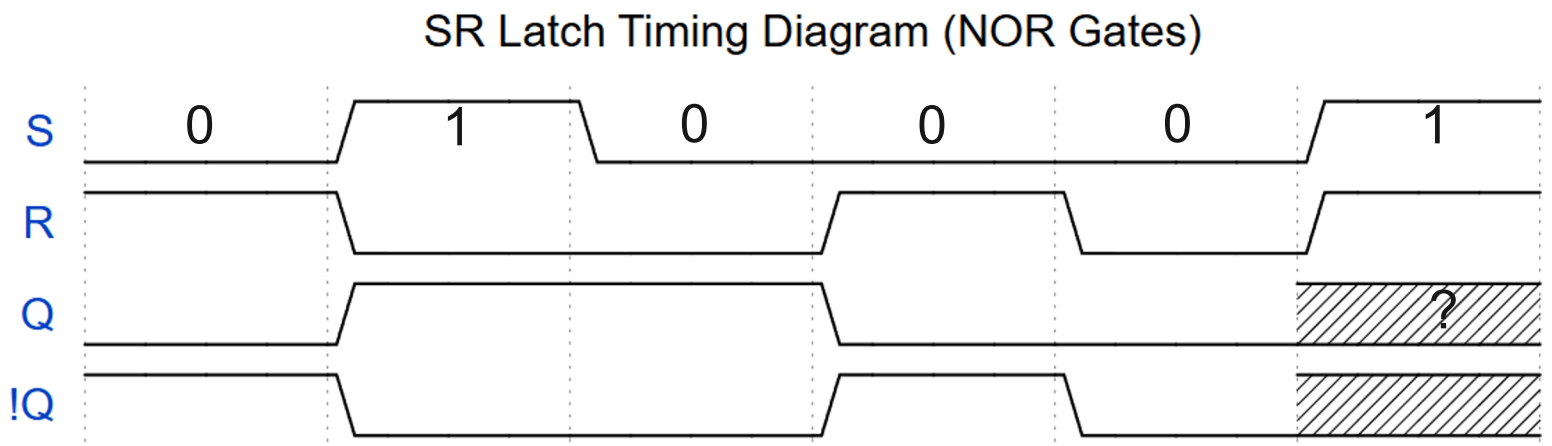
Understanding and coding! a timing diagram

SR latch truth table

S	R	Output (Q)
0	0	**Previous State**
0	1	**0**
1	0	**1**
1	1	**0 (Invalid)**

https://wavedrom.com/

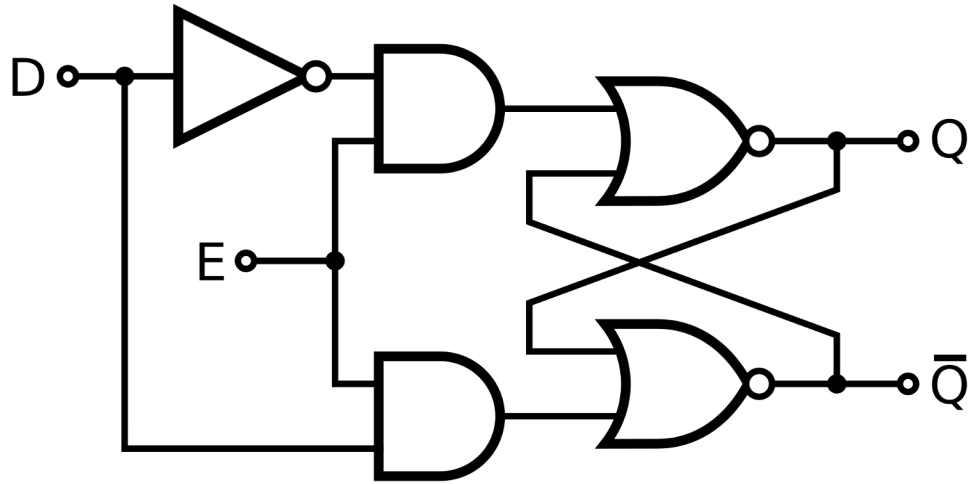
```
{
  "signal": [
    {"name": "S",        "wave": "010..1"},
    {"name": "R",        "wave": "10.101"},
    {"name": "Q",        "wave": "01.0.?"},
    {"name": "!Q", "wave": "10.10?"}
  ],
  "head": {
    "text": "SR Latch Timing Diagram (NOR Gates)"
  },

  "config": {
    "hscale": 2
  }
}
```



COE COLLEGE

A latch with a “single” input

A gated D latch

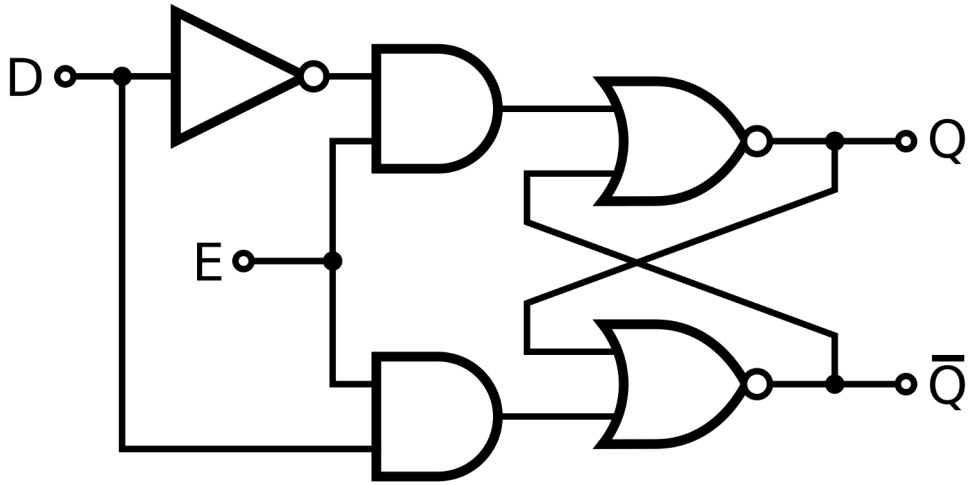


https://en.wikipedia.org/wiki/Flip-flop_(electronics)

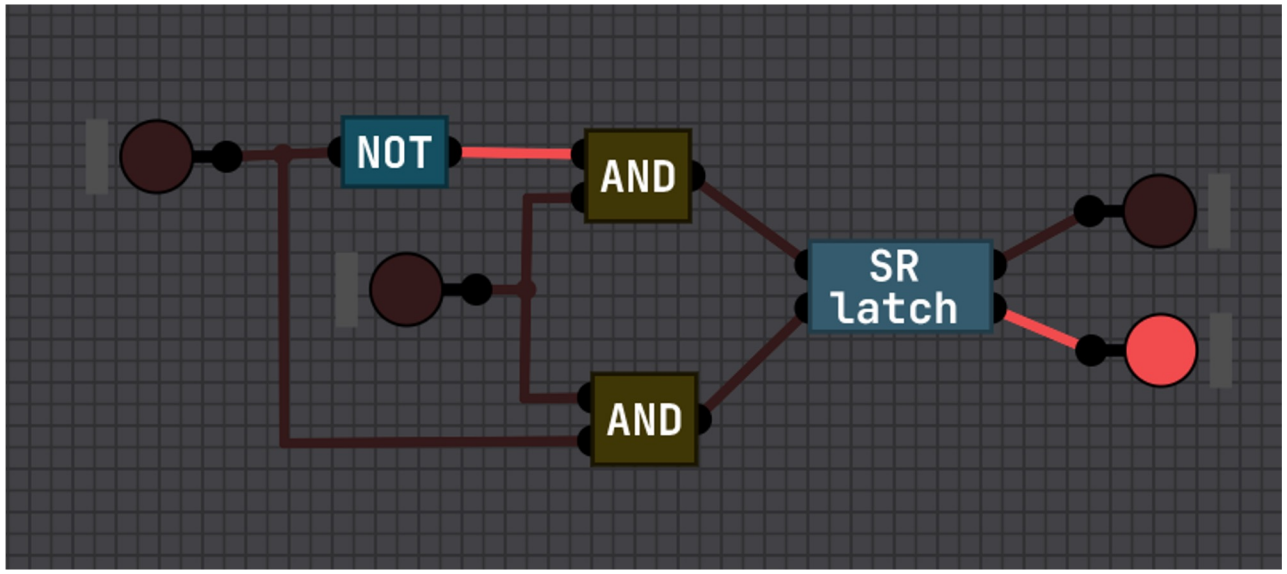
COE COLLEGE

A latch with a “single” input

A gated D latch



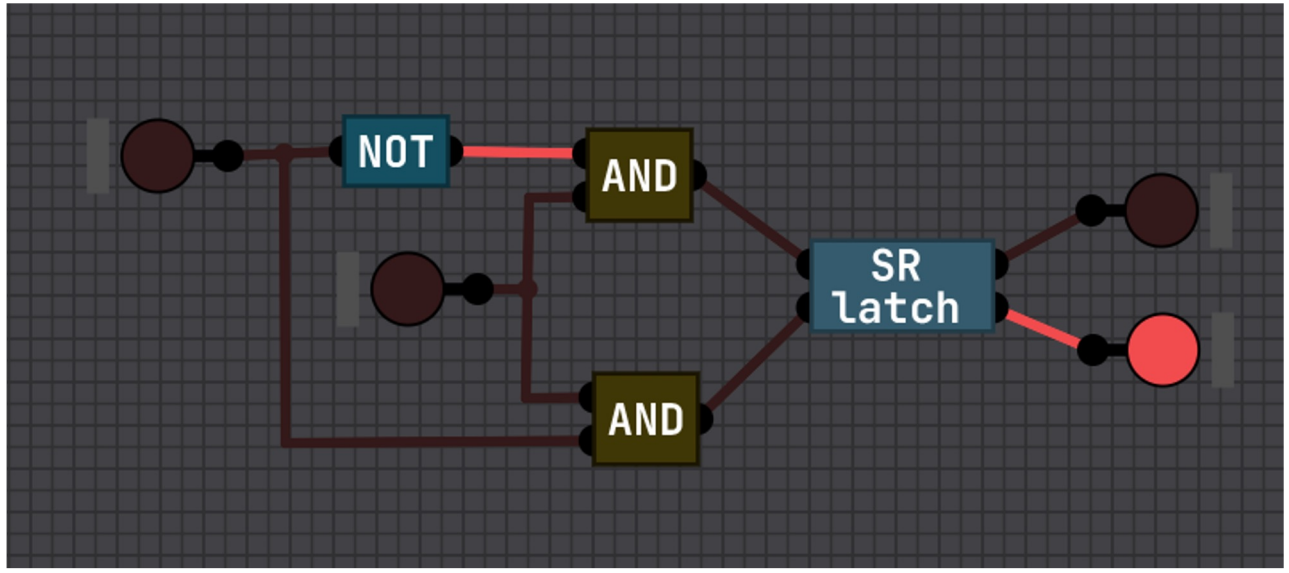
https://en.wikipedia.org/wiki/Flip-flop_(electronics)



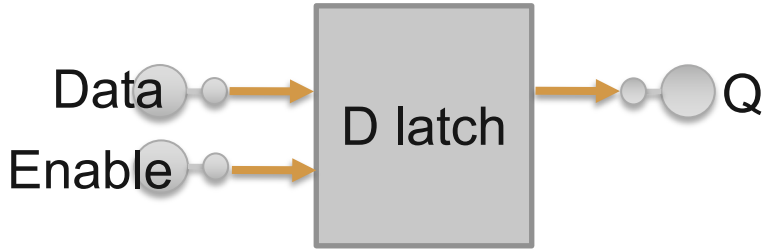
COE COLLEGE

A latch with a “single” input

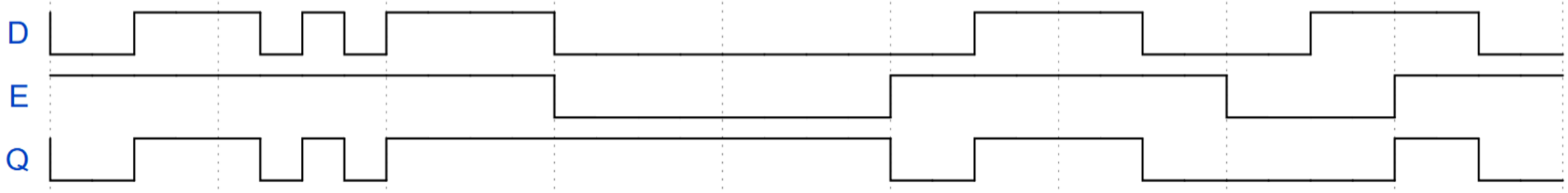
A gated D latch



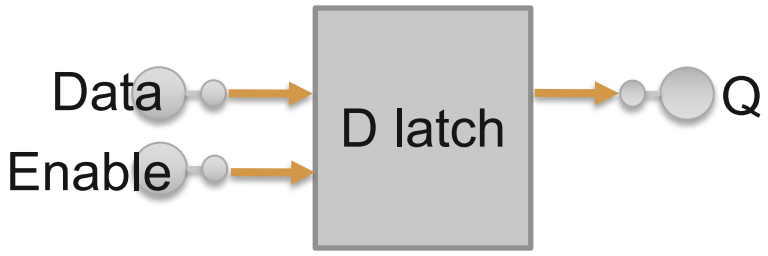
Also known as: D latch/data latch



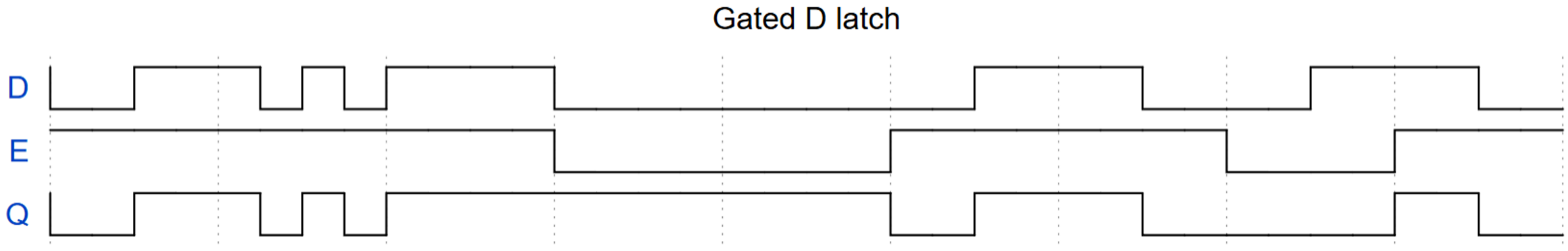
Gated D latch



D latch timing diagram code

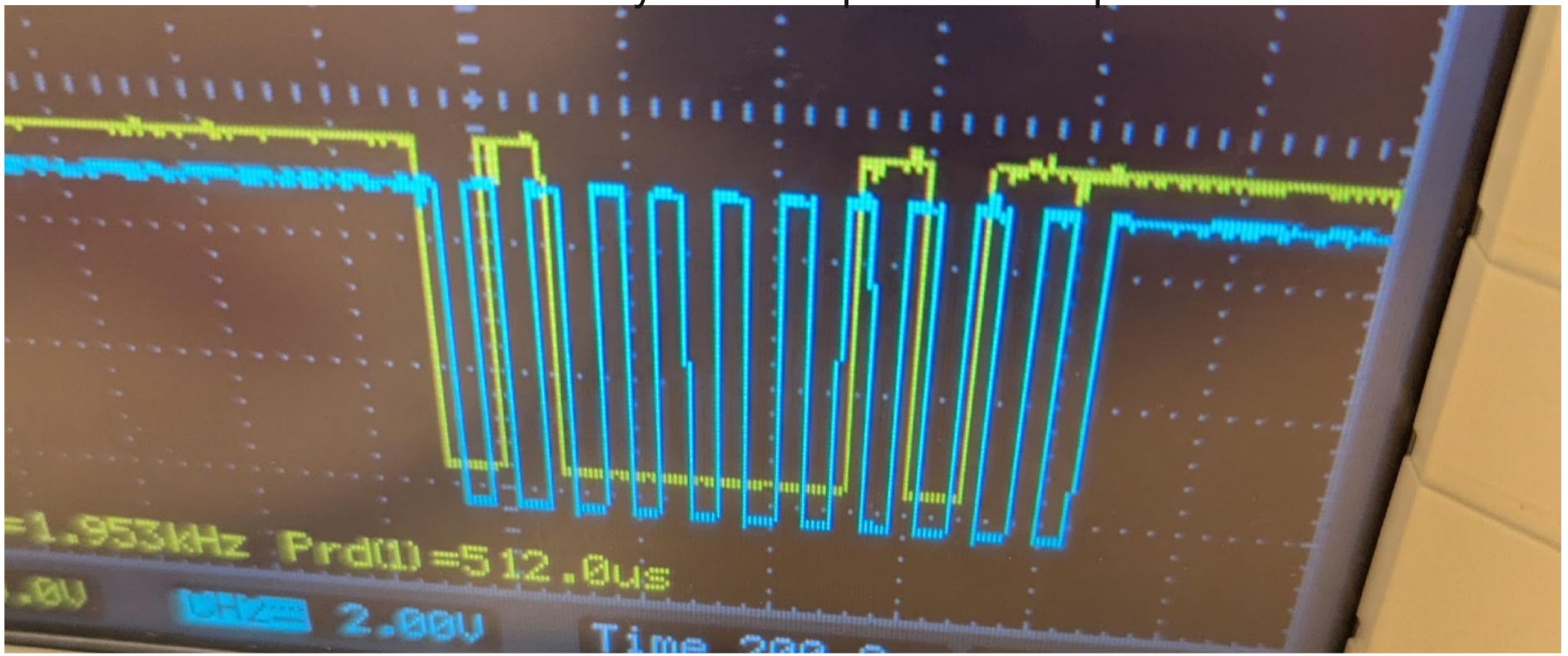



```
{
  "signal": [
    {"name": "D",       "wave": "n<hlhl>hl.n<h.l..h..l."},
    {"name": "E",       "wave": "h..l.h.lh"},
    {"name": "Q",       "wave": "n<hlhl>h..n<h.l...h.l."},

  ],
  "head": {
    "text": "Gated D latch"
  },

  "config": {
    "hscale": 2
  }
}

```



Let’s practice timing diagrams!

11-bits keyboard output via PS/2 port:



COE COLLEGE

Let's practice timing diagrams!

Turn this truth table into a timing diagram!

A \ BC	00	01	11	10
0	**0**	**1**	**1**	**1**
1	**1**	**1**	**1**	**0**

COE COLLEGE

Let’s practice timing diagrams!

Turn this Hamming encoding into a timing diagram!

Data: 01010101010

Adding P1:
Adding P2:
Adding P3:
Adding P4:
Adding P0:

Code:

```
{ "signal" : [
  { "name": "Input",  "wave": "01010101010", node: 'abcdefghijk' },
  {},
  {},
  {},
  { "name": "Parity check 1",  "wave": "x1x0x101x0101010", node: '.p.............' },

],
  edge: [
  'a->p','b->p','d~>p','e~>p','g~->p','i~->p','k~->p'
  ]

  }
```